| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/671,303 | BAO ET AL. | |
| | Examiner | Art Unit | |
| | Bradley K. Smith | 2891 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-18, 27-40*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Brad Smith
Primary Examiner

**EXAMINER'S AMENDMENT**

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jay Brown on 1/20/06.

The application has been amended as follows:

In the Claims:

Please amend the claims as follows:

1. (Currently amended) A semiconductor apparatus, comprising:

a substrate having a substrate surface;

a layer of a first material overlying a first region of said substrate surface;

a layer of a second material overlying a second region of said substrate surface;

a layer of a semiconductor overlying said layer of first material and overlying said layer of second material ~~a second region of said substrate surface~~; and

a first region of said layer of semiconductor ~~semiconductor,~~ overlying said layer of first material and including crystal grains having a first average crystal grain ~~size;~~ size, a second region of said layer of semiconductor ~~semiconductor,~~ overlying said layer of second material ~~second region of said substrate surface~~ and including crystal grains having a second average crystal grain ~~size; and~~ size, said first average crystal grain size being substantially different from said second average crystal grain size.

2. (Currently amended) A semiconductor apparatus, comprising:

a substrate having a substrate surface;

a layer of a first material overlying a first region of said substrate surface;

a layer of a second material overlying a second region of said substrate surface;

a layer of a semiconductor overlying said layer of first material and overlying said layer of second material ~~a second region of said substrate surface~~; and

a first region of said layer of semiconductor ~~semiconductor,~~ overlying said layer of first material and having a first conductivity, ~~conductivity;~~ a second region of said layer of semiconductor ~~semiconductor,~~ overlying said layer of second material ~~second region of said substrate surface~~ and having a second conductivity, ~~conductivity; a layer of a second material overlying said second region of said substrate surface, said second region of said layer of semiconductor overlying said layer of said second material; and~~ said first conductivity being substantially different from said second conductivity.

3. (Original) The semiconductor apparatus of claim 1, in which said first material is a polymer.

4. (Currently amended) The semiconductor apparatus of claim 1, in which:

said first region of said layer of semiconductor has a first conductivity;

said second region of said layer of semiconductor has a second conductivity; and

said first conductivity is at least about 100 times as large as said second conductivity.

5. (Previously presented) The semiconductor apparatus of claim 1, in which said first average crystal grain size is at least about 10 times as large as said second average crystal grain size.

6. (Currently amended) The semiconductor apparatus of claim 1, in which an ~~the~~ average separation between crystal grains within said second region of said layer of

semiconductor is at least about 10 times as large as an ~~the~~ average separation between crystal grains within said first region of said layer of semiconductor.

7. (Original) The semiconductor apparatus of claim 1, in which said semiconductor is selected from the group consisting of: acenes, thiophenes, bithiophenes, phthalocyanines, naphthalene-1,4,5,8-tetracarboxylic diimide compounds, naphthalene-1,4,5,8-tetracarboxylic dianhydride, and 11,11,12,12-tetracyanonaphtho-2,6-quinodimethane.

8. (Original) The semiconductor apparatus of claim 1, further comprising:

a first gate electrode;

a first source electrode; and

a first drain electrode;

said first source and drain electrodes being in spaced apart conductive contact with a first channel portion of either said first or said second region of said layer of semiconductor, said first gate electrode being positioned to control a conductivity of said first channel portion.

9. (Original) The semiconductor apparatus of claim 2, in which said layer of first material overlies said second region of said substrate surface.

10. (Currently amended) The semiconductor apparatus of claim 1 ~~claim 2~~, in which said second material is a polymer.

11. (Currently amended) The semiconductor apparatus of claim 3 ~~claim 2~~, in which said first material is selected from the group consisting of: poly(para-vinyl phenol), poly(4-vinylpyridine), poly(2-vinylnaphthalene), poly(meta-vinyl phenol), poly(ortho-vinyl phenol), poly(para-vinyl phenol)-co-2-hydroxyethylmethacrylate [[poly(para-vinyl phenol)-co-2-hydroxyethylmethac- rylate]], poly(2-vinylpyridine), poly(2-vinylnaphthalene-co-2-ethylhexyl acrylate, poly(1-vinylnaphthalene), and blends.

12. (Currently amended) A semiconductor apparatus, comprising:

a substrate having a substrate surface;

a layer of a first material overlying a first region of said substrate surface;

a layer of a semiconductor overlying said layer of first material and overlying a second region of said substrate surface;

a first region of said layer of semiconductor ~~semiconductor,~~ overlying said layer of first material and having a first conductivity, ~~conductivity;~~ a second region of said layer of semiconductor ~~semiconductor,~~ overlying said second region of said substrate surface and having a second conductivity, ~~conductivity; and~~ said first conductivity being substantially different from said second conductivity;

first and second gate electrodes;

first and second source electrodes; and

first and second drain electrodes;

said first source and first drain electrodes being in spaced apart conductive contact with a first channel portion of either said first region or said second region of said layer of

semiconductor, said first gate electrode being positioned to control a conductivity of said first channel portion;

said second source and second drain electrodes being in spaced apart conductive contact with a second channel portion of either said first region or said second region of said layer of semiconductor, said second gate electrode being positioned to control a conductivity of said second channel portion;

wherein said first and second channel portions are mutually isolated by an interposed region of said layer of semiconductor having a substantially lower conductivity than said conductivity of said first and second channel portions.

13. (Original) The semiconductor apparatus of claim 10, in which said second material is selected from the group consisting of: poly(n-butyl methacrylate), poly(vinylidene difluoride-co-methyl vinyl ether), polystyrene, poly(p-methoxystyrene), poly(vinylidene difluoride), poly(vinyl acetate), poly(vinyl propionate), poly(methoxy acetate), poly(n-propyl methacrylate), poly(isopropyl methacrylate), poly(n-pentyl methacrylate), poly(vinylidene difluoride-co-ethyl vinyl ether), poly(vinylidene difluoride-co-propyl vinyl ether), poly(dimethylaminoethyl methacrylate), poly(dimethylaminopropyl methacrylate), poly(aminopropyl methacrylate), poly(diethylaminoethyl methacrylate), and blends.

14. (Original) The semiconductor apparatus of claim 10, in which said second material comprises charge carrier traps.

15. (Original) The semiconductor apparatus of claim 11, in which said first material comprises poly(4-vinylpyridine).

16. (Original) The semiconductor apparatus of claim 11, in which said first material comprises poly(2-vinylnaphthalene).

17. (Currently amended) The semiconductor apparatus of claim 13, in which said second material comprises poly(n-butyl ~~butyl~~ methacrylate).

18. (Currently amended) The semiconductor apparatus of claim 13, in which said second material comprises poly(vinylidine difluoride~~fluoride~~ co-methyl vinyl ether).

19-26. (Cancelled)

27. (Cancelled)

28. (Previously presented) The semiconductor apparatus of claim 1, in which said layer of first material overlies said second region of said substrate surface.

29. (Currently amended) The semiconductor apparatus of claim 2 ~~claim 27~~, in which said second material is a polymer.

30. (Previously presented) The semiconductor apparatus of claim 2, in which said first material is a polymer.

31. (Previously presented) The semiconductor apparatus of claim 2, in which said first conductivity is at least about 100 times as large as said second conductivity.

32. (Currently amended) The semiconductor apparatus of claim 2, in which said layer of semiconductor comprises crystal grains, and in which an ~~the~~ average crystal grain size within said first region of said layer of semiconductor is at least about 10 times as large as an ~~the~~ average crystal grain size within said second region of said layer of semiconductor.

33. (Previously presented) The semiconductor apparatus of claim 12, further comprising a layer of a second material overlying said second region of said substrate surface, said second region of said layer of semiconductor overlying said layer of said second material.

34. (Previously presented) The semiconductor apparatus of claim 12, in which said layer of first material overlies said second region of said substrate surface.

35. (New) A semiconductor apparatus, comprising:

a substrate having a substrate surface;

a layer of a first material overlying a first region of said substrate surface;

a layer of a second material overlying a second region of said substrate surface;

a layer of a semiconductor overlying said layer of first material and overlying said layer of second material; and

a first region of said layer of semiconductor overlying said layer of first material and including crystal grains having a first average crystal grain size, a second region of said layer of semiconductor overlying said layer of second material and including crystal grains having a second average crystal grain size, said first average crystal grain size being substantially larger than said second average crystal grain size.

36. (New) The semiconductor apparatus of claim 35, in which said first average crystal grain size is at least about 10 times as large as said second average crystal grain size.

37. (New) The semiconductor apparatus of claim 35, in which an average separation between crystal grains within said second region of said layer of semiconductor is at least about 10 times as large as an average separation between crystal grains within said first region of said layer of semiconductor.

38. (New) The semiconductor apparatus of claim 35, in which:

said first region of said layer of semiconductor has a first conductivity;

said second region of said layer of semiconductor has a second conductivity; and

said first conductivity is at least about 100 times as large as said second conductivity.

39. (New) The semiconductor apparatus of claim 35, further comprising:

a first gate electrode;

a first source electrode; and

a first drain electrode;

said first source and drain electrodes being in spaced apart conductive contact with a first channel portion of either said first region or said second region of said layer of semiconductor, said first gate electrode being positioned to control a conductivity of said first channel portion.

40. (New) The semiconductor apparatus of claim 35, in which said layer of first material overlies said second region of said substrate surface.

The following is an examiner's statement of reasons for allowance: the prior art of record neither teaches nor suggests the formation of a first and a second material with a layer of semiconductor material overlying the first and second material, the first region of the semiconductor layer overlying the first material has a first crystal grain size and the second material overlying the second layer has a second crystal grain size, and the two sizes being substantially different.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bradley K. Smith whose telephone number is 571-272-1884. The examiner can normally be reached on 10-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bradley K Smith
Primary Examiner
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